广 东 东 邦 科 技 有 限 公 司

GUANG DONG DONGBOND TECHNOLOGY CO., LTD.

SPECIFICATIONS FOR LCD MODULE

FOR CUSTOMER	
LCD MODEL	DBT040TS02A
CUSTOMER APPROVED	

PREPARED BY	CHECKED BY	APPROVED BY	DATE
唐超凡	隆茂生	周国正	**13.09.23**

■**Preliminary Specification**
□**Final Specification**

Note : All Materials And The Craft Must Conform To The RoHS Environmental Protection Requirement

广东省深圳市高新技术产业园北区朗山一路 8 号
No.8 Langshan Road 1,hi-tech industrial Park North, Nanshan District Shenzhen,Guandong,PRC
电话/Tel: 0755-26501518 传真/Fax: 0755-26501718 邮编/P.C.: 518057

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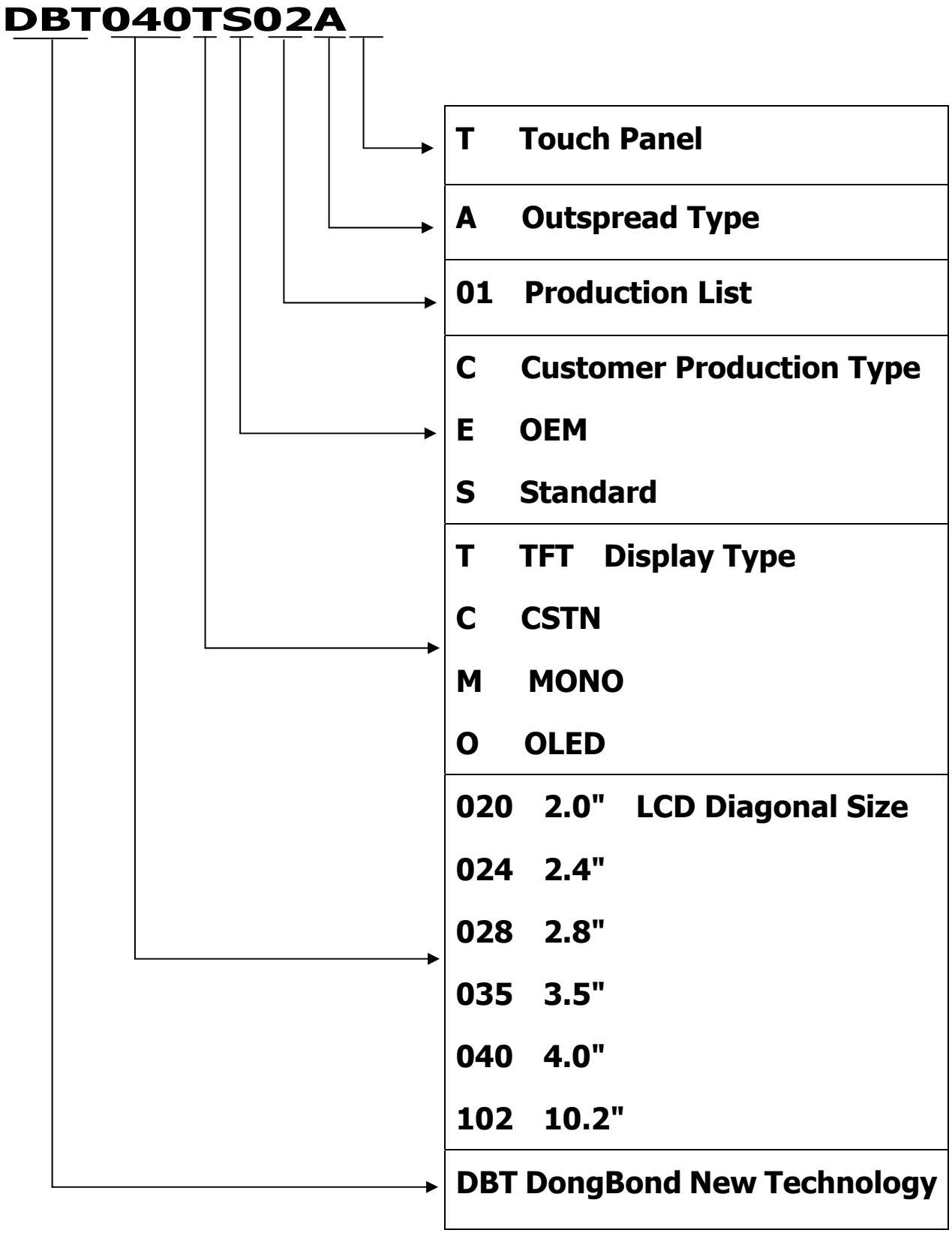
2. Revision History

Version	Content	Page	Date
A0	Generation first version		2013-09-23

Note : The Product and specifications are subject to change without any notice. Please ask for the latest Product Standards to guarantee the satisfaction of our product requirements.

3. Numbering System



4. PRODUCT INFORMATION

4.1. Description

DBT040TS02A is a color active matrix LCD module incorporating amorphous silicon TFT(Thin Film Transistor). It is composed of a color TFT-LCD panel, driver ICs, FPC and a backlight unit. The 4.0″ display area contains 480(RGB) x 800pixels and can display up to 17.6M colors.

4.2. Applications

- ☐ **UMPC**
- ☐ **Digital photo frame**
- ☐ **GPS**

4.3. Features

- ☐ **High Resolution: 480(RGB) x 800 Dots**
- ☐ **Panel Size:4.0(16:9 diagonal) inch**
- ☐ **Interface: MIPI**
- ☐ **7 LED backlight**

4.4. General Specifications

Item	Specification	Unit	Remark
Display Mode	Normally White	-	-
Display Technology	α-Si TFT active matrix	-	-
Outline Dimension	57.24(H) X 98.3(V) X2.05(T)	mm	-
Active Area	86.40(H) X51.84 (V)	mm	-
Resolution	480X(RGB)X800	dots	-
Pixel Pitch	108X108	μm	-
Pixel Configuration	RGB Stripe	-	-
Weight	TBD	g	-
Luminance	350（TYP）	cd/m2	-
Signal Interface	MIPI	-	-
Viewing Direction	MVA	o'clock	Note

5. ABSOLUTE MAXIMUM RATINGS

GND=0V, Ta = 25℃

Item	Symbol	MIN	MAX	Unit	Remark
Logic Supply Voltage	IOVCC	-0.3	3.6	V	
Analog Supply Voltage	VCC	-0.3	5.5	V	
Input voltage	CS/RS/WR/RD /D0~D23	-0.3	IOVCC+0.5	V	
Back Light Forward Current	I_F	-	25	mA	ONE LED
Operating Temperature	Top	-20	70	℃	
Storage Temperature	Tst	-30	80	℃	

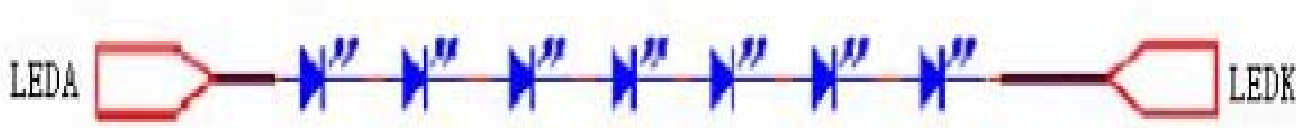
6. ELECTRICAL SPECIFICATIONS(Ta=25°C)

6.1. DC CHARACTERISTICS

DND=0V,Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage	VCI	2.3	2.8	4.8	V	
Supply Voltage	IOVCC	1.65	2.8	3.3	V	
High-level Input Voltage	VI	0.7* IOVCC	-	IOVCC	V	
Low-level Input Voltage	VI	0	-	0.3* IOVCC	V	
High-level Output Voltage	VO	0.8* IOVCC	-	IOVCC	V	IOH=+1.0mA
Low-level Output Voltage	VO	0	-	0.2* IOVCC	V	IOL=-1.0mA
Supply Current for	IF	-	20	-	mA	

6.2. Backlight Driving Section



6.3. BACKLIGHT CHARACTERISTICS

Ta=25℃

Item	Symbo	MIN	TYP	MAX	Unit	Remark
LED Current	I_F	--	20	--	mA	For each LED
LED Voltage	V_F	2.8	3.2	3.4	V	For each LED
LED Consumption	W_{BL}	--	64	--	mW	For each LED

7. OPTICAL SPECIFICATIONS(Ta=25℃)

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Contrast Ratio		C/R	-	600	-		Fig.1
Brightness		-	300	350	-	cd/m2	Full White Pattern (Transmittance 7.4%)
Brightness Uniformity			70	-	-	%	Full White Pattern
Response Time		Tr+Tf	-	20	-	ms	Fig.3
Color Coordinate	WHITE	Wx	0.270	0.30	0.330		IBL=20mA Full White Pattern
		Wy	0.297	0.327	0.357		
view angle		θl	75	80	-	Degree	Fig.4 Center (C/R>10)
		θr	75	80	-		
		θu	75	80	-		
		θd	75	80	-		

Note:

1. Contrast Ratio(CR) is defined mathematically as :

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

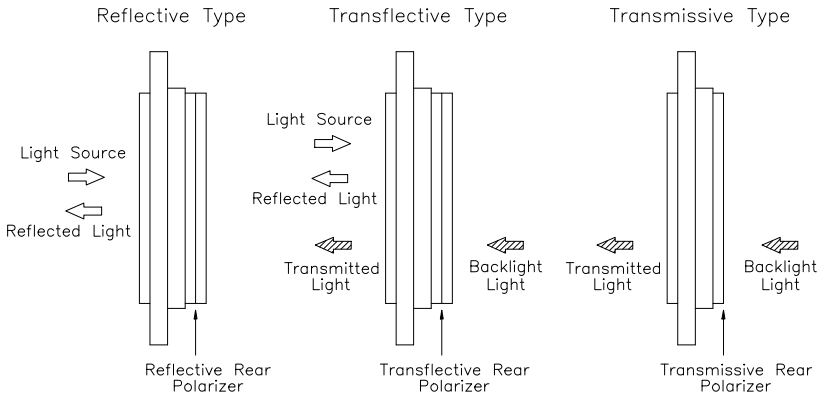
2. Surface luminance is the center point across the LCD surface 500mm from the surface with all pixels displaying white. For more information see FIG 1.

3. Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black(Decay Time, Tf). For additional information see FIG 3.

4. Viewing angle is the angle at which the contrast ratio is greater than 5. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 4.

5. Optimum contrast is obtained by adjusting the LCD Threshold voltage (Vth& Vsat)

8. Viewing Modes



9. Electro-Optical Characteristics Test Method

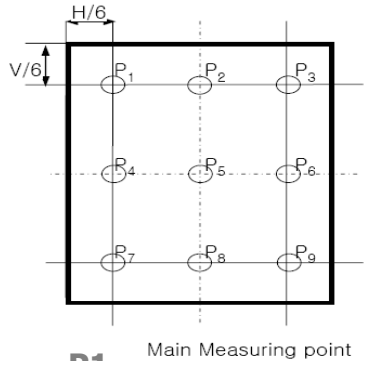


Fig. 2 Measuring Points

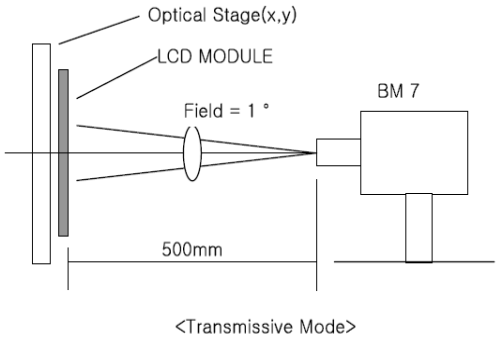


FIG. 1 Optical Characteristic Measurement Equipment and Method

The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white".

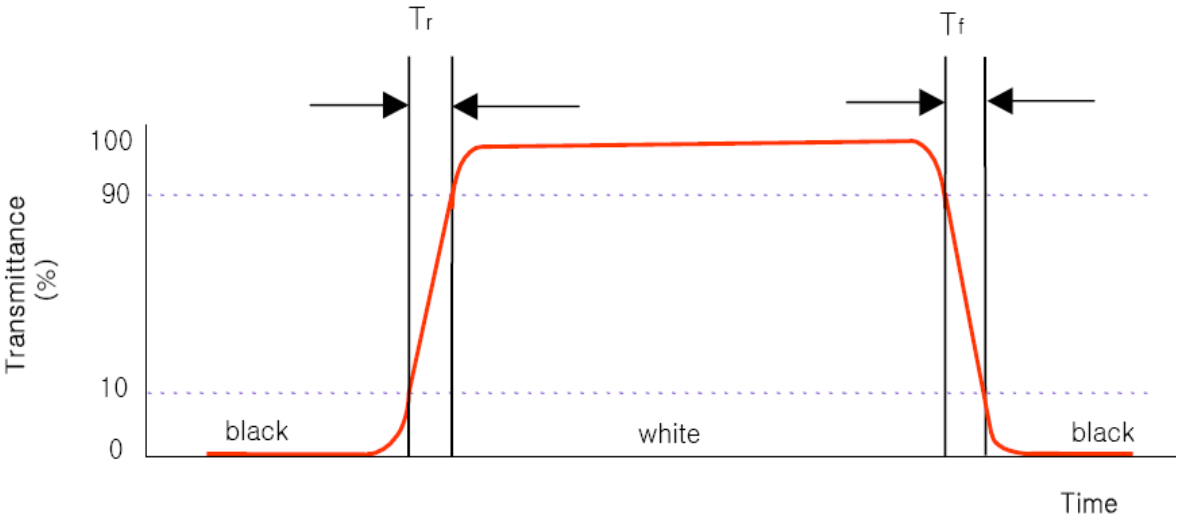


FIG.3 The definition of Response Time

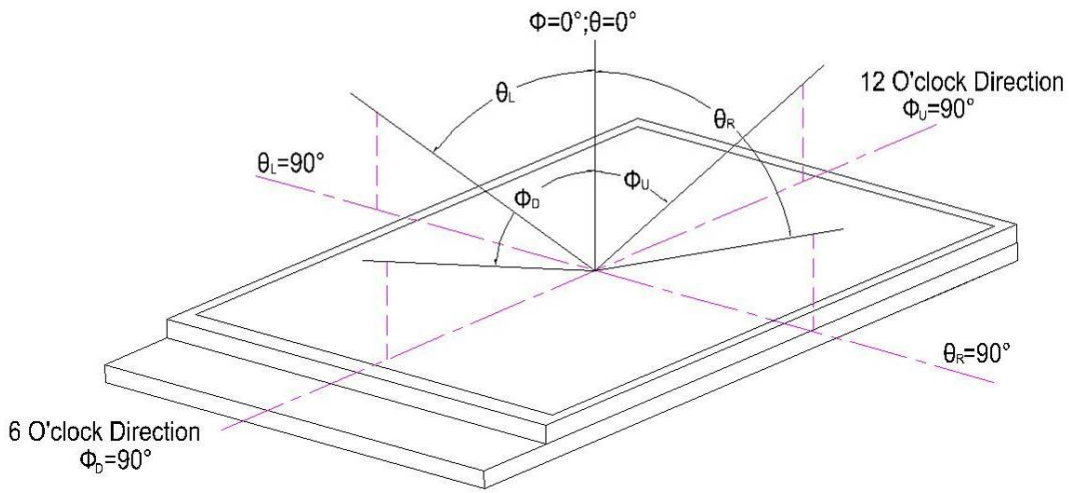
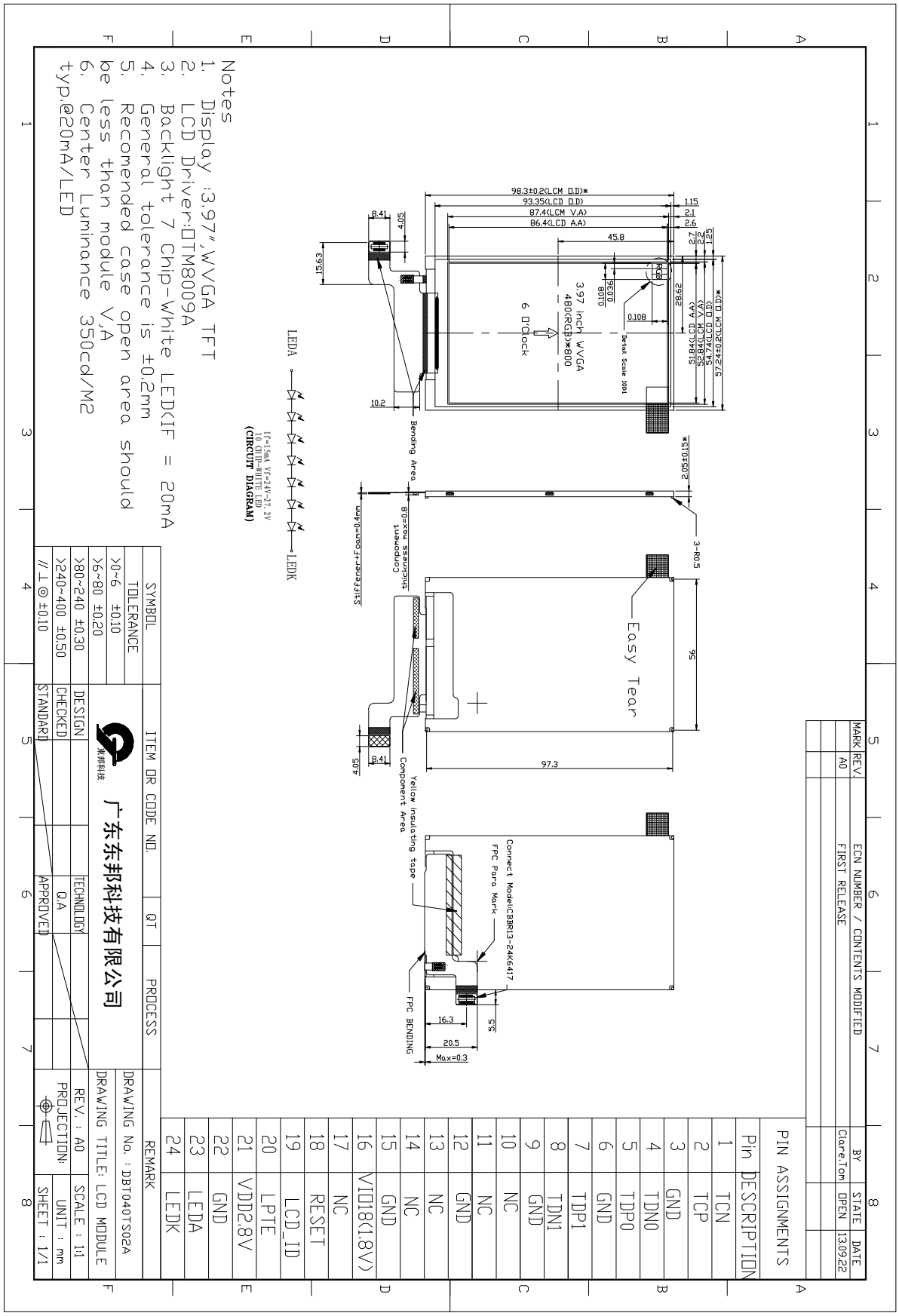
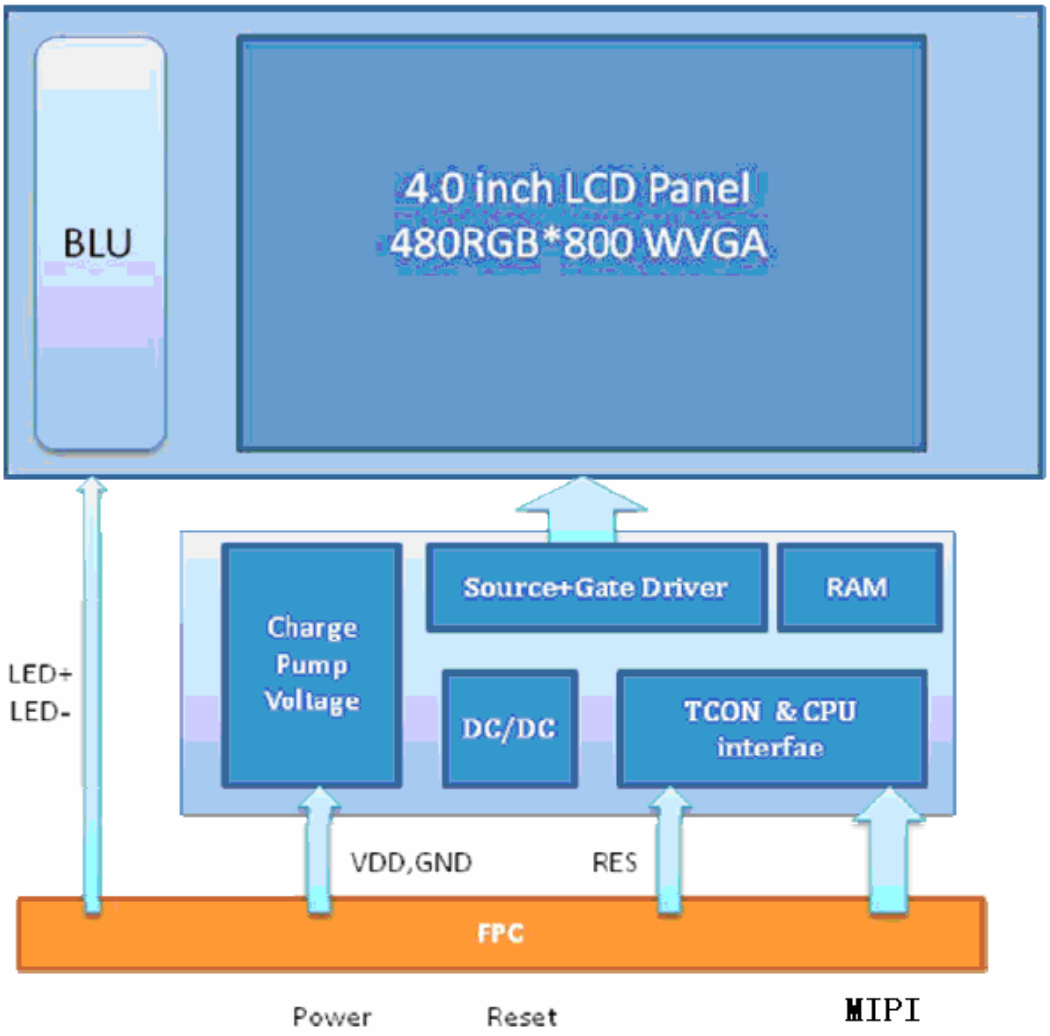


FIG.4 The definition of Viewing Angle

10. <Outline dimension>



11. <Block diagram>



12. <Table of Pin Assignment >

LCM Pin Assignment

Pin No.	Symbol	I/O	Description	Remark
1	TCN	I	MIPI-DSI Clock Lane Negative	
2	TCP	I	MIPI-DSI Clock Lane Positive	
3	GND	P	ground	
4	TDN0	I	MIPI-DSI Data Lane Negative 0	
5	TDP0	I	MIPI-DSI Data Lane Positive 0	
6	GND	P	ground	
7	TDN1	I	MIPI-DSI Data Lane Negative 1	
8	TDP1	I	MIPI-DSI Data Lane Positive 1	
9	GND	P	ground	
10	NC	-	No Connect	
11	NC	-	No Connect	
12	GND	P	ground	
13	NC	-	No Connect	
14	NC	-	No Connect	
15	GND	P	ground	
16	VDDIO	I	I/O PWOER	
17	NC	I	No Connect	
18	RESET	I	RESET Signal	
19	LCD_ID	I	LCD_ID	
20	LPTE	O	Tearing effect output pin	
21	VDD2.8V	I	Power Supply	
22	GND	P	ground	
23	LEDA	I	LABAR Positive	
24	LEDK	I	LABAR Negative	

Note 1: I/O---Input/Output; I---Input; P---Power/Ground

13. <MIPI-DSI interface>

13.1. General description

The communication can be separated 2 different levels between the MCU and the display module

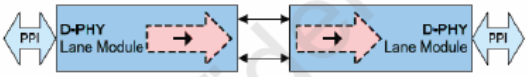
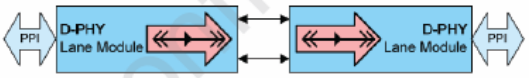
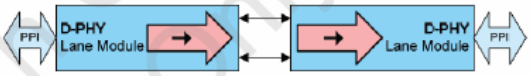
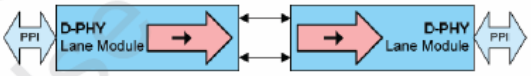
-Interface Level: Low level communication

-Packet level: High level communication

13.2. Interface level communication

13.3.General

The display module uses data and clock lane differential pairs for DSI. Both clock lane and data lane0 can driven Low Power(LP)or High Speed(HS)mode. Data lane1 and Data lane2 can be driven High speed mode only.

	Lane support mode	MPU(Host) OTM8009A(Slave)
Clock Lane	Unidirectional lane ★High-Speed Clock only ★Simplified Escape Mode (ULPS Only)	
Data lane0	Bi-directional lane ★Forward high-speed only ★Bi-directional Escape Mode ★Bi-direction LPDT	
Data lane1	Unidirectional lane ★Forward high-speed only ★Simplified Escape Mode (ULPS Only)	
Data lane2	Unidirectional lane ★Forward high-speed only ★Simplified Escape Mode (ULPS Only)	

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable)and it can be driven into a low power mode.

High Speed mode means that different modes and protocols in each mode when there are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to the display module and vice versa.

The state Codes of the High Speed (HS)and Low Power(LP)lane pair are defined below.

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low-Power (LP)	
	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

14. Reliability

Item NO.	Test Item	Test condition	Description
1	**High temperature operation**	**Ta=70℃,240 h**	**Endurance test applying the electric operation under high temperature for a long time**
2	**Low temperature operation**	**Ta=-20℃,240 h**	**Endurance test applying the electric operation under low temperature for a long time**
3	**High temperature storage**	**Ta=80℃,240 h**	**Endurance test applying the high storage temperature for a long time**
4	**Low temperature storage**	**Ta=-30℃,240 h**	**Endurance test applying the low storage temperature for a long time**
5	**High temperature High humidity**	**Ta=60℃, 90%RH,240 h**	**Endurance test applying electric operation under high temperature and high humidity for a long time**
6	**Temperature Cycle**	**-30℃(30min), +80℃(30min) 200cycles**	**Endurance test applying the low and high temperature cycle** **One cycle**
7	**Shock Test**	**100G ,6ms Direction: X,Y,Z 3 times**	**Measure an aerospace product's response to mechanical shock**

15. packaging

TBD